CLAIMS

1. An electronic device, comprising:

a memory structure comprising an integer M of word storage locations;

a write shift register for storing a sequence of bits, wherein the sequence in the write shift register comprises a number of bits equal to a ratio of $1/R_1$ times the integer M;

circuitry for providing a write clock cycle to the write shift register for selected write operations with respect to any of the word storage locations;

wherein in response to each write clock cycle, received from the circuitry for providing the write clock cycle, the write shift register shifts the sequence in the write shift register;

wherein one bit in the sequence in the write shift register corresponds to an indication of one of the memory word storage locations into which a word will be written;

a read shift register for storing a sequence of bits, wherein the sequence in the read shift register comprises a number of bits equal to a ratio of $1/R_2$ times the integer M;

circuitry for providing a read clock cycle to the read shift register for selected read operations with respect to any of the word storage locations;

wherein in response to each read clock cycle, received from the circuitry for providing the read clock cycle, the read shift register shifts the sequence in the read shift register;

wherein one bit in the sequence in the read shift register corresponds to an indication of one of the memory word storage locations from which a word will be read; and

circuitry for evaluating selected bits in the sequence in the write register relative to selected bits in the sequence in the read register for detecting a level of data fullness in the memory structure.

2. The device of claim 1 wherein R_1 equals R_2.

3. The device of claim 2 wherein R_1 and R_2 both equal one.

4. The device of claim 1:

wherein the circuitry for providing a write clock cycle to the write shift register for selected write operations provides a write clock cycle for every R_1 write operations with respect to any of the word storage locations; and

wherein the circuitry for providing a read clock cycle to the read shift register for selected read operations provides a read clock cycle for every R_2 read operations with respect to any of the word storage locations.

5. The device of claim 1 wherein the circuitry for evaluating selected bits comprises circuitry for monitoring positioning of the sequence in the write shift register relative to positioning of the sequence in the read shift register.

6. The device of claim 5 wherein the circuitry for evaluating provides a signal in response to detecting that the positioning of the sequence in the write shift register is approaching the positioning of the sequence in the read shift register so as to indicate that the M storage locations are approaching a data full status.

7. The device of claim 5 wherein the circuitry for evaluating provides a signal in response to detecting that the positioning of the sequence in the read shift register is approaching the positioning of the sequence in the write shift register so as to indicate that the M storage locations are approaching a data empty status.

8. The device of claim 5 wherein the circuitry for evaluating provides a signal in response to detecting that the positioning of the sequence in the write shift register relative to the positioning of the sequence in the read shift register indicates that the one of the memory word storage locations into which a word will be written is $M/2$ storage locations away from the one of the memory word storage locations from which a word will be read.

9. The device of claim 8:

wherein the sequence in the write shift register comprises three contiguous bits of a first binary value and a plurality of contiguous bits of a second binary value that is complementary to the first binary value; and

wherein the sequence in the read shift register comprises three contiguous bits of the first binary value and a plurality of contiguous bits of the second binary value.

10. The device of claim 9 wherein the circuitry for evaluating comprises an AND gate having an input coupled to a selected bit location in the read shift register and having an input coupled to a selected bit location in the write shift register, wherein the selected bit locations in the read and write shift registers are at a distance of $M/2$ locations from one another.

11. The device of claim 9 wherein the circuitry for evaluating comprises:

an AND gate having an input coupled to a selected bit location in the read shift register and having an input coupled to a selected like bit location in the write shift register; and

circuitry for evaluating a data state in the read shift register at a bit location located at two lesser significant locations relative to the selected bit location in the read shift register.

12. The device of claim 1:

wherein the sequence in the write shift register comprises two contiguous bits of a first binary value and a plurality of contiguous bits of a second binary value that is complementary to the first binary value; and

wherein the sequence in the read shift register comprises two contiguous bits of the first binary value and a plurality of contiguous bits of the second binary value.

13. The device of claim 12 wherein the circuitry for evaluating comprises an AND gate having an input coupled to a selected bit location in the read shift register and having an input coupled to a selected bit location in the write shift register, wherein the selected bit locations in the read and write shift registers are at a same relative bit location in each of the read and write shift registers.

14. The device of claim 13 wherein the circuitry for evaluating further comprises circuitry for evaluating a binary value in one of the write or read shift register at a bit location immediately following, with respect to shifting direction, the selected bit location.

15. The device of claim 1:

wherein the sequence in the write shift register comprises three contiguous bits of a first binary value and a plurality of contiguous bits of a second binary value that is complementary to the first binary value; and

wherein the sequence in the read shift register comprises three contiguous bits of the first binary value and a plurality of contiguous bits of the second binary value.

16. The device of claim 15 wherein the circuitry for evaluating comprises:

an AND gate having an input coupled to a selected bit location in the read shift register and having an input coupled to a selected bit location in the write shift register, wherein the selected bit locations in the read and write shift registers are at a same relative bit location in each of the read and write shift registers; and

circuitry for evaluating a value in one of the write or read shift register at a bit location spaced two bit locations, with respect to shifting direction, from the selected bit location.

17. The device of claim 1 wherein each of the write shift register and the read shift register comprises a wraparound shift register.

18. The device of claim 1 wherein the circuitry for evaluating provides a signal indicating the level of data fullness in the memory structure in response to a single logic gate connected to a single bit in the read shift register and a single bit in the write shift register.

19. The device of claim 1:

wherein one bit in the sequence in the write shift register corresponds to an indication of one of the memory word storage locations into which a word will be written by providing a write pointer to the one of the memory word storage locations into which a word will be written; and

wherein one bit in the sequence in the read shift register corresponds to an indication of one of the memory word storage locations from which a word will be read by providing a read pointer to the one of the memory word storage locations from which a word will be read.

20. The device of claim 1:

wherein one bit in the sequence in the write shift register corresponds to an indication of one of the memory word storage locations into which a word will be written by tracking a write pointer that indicates the one of the memory word storage locations into which a word will be written; and

wherein one bit in the sequence in the read shift register corresponds to an indication of one of the memory word storage locations from which a word will be read by tracking a read pointer that indicates the one of the memory word storage locations from which a word will be read.

21. A method of operating an electronic device, the electronic device comprising a memory structure comprising an integer M of word storage locations, the method comprising:

storing a sequence of bits in a write shift register, wherein the sequence in the write shift register comprises a number of bits equal to a ratio of $1/R_1$ times the integer M;

providing a write clock cycle to the write shift register for selected write operations with respect to any of the word storage locations;

in response to each write clock cycle, received from the circuitry for providing the write clock cycle, shifting the sequence in the write shift register;

wherein one bit in the sequence in the write shift register corresponds to an indication of one of the memory word storage locations into which a word will be written;

storing a sequence of bits in a read shift register, wherein the sequence in the read shift register comprises a number of bits equal to a ratio of $1/R_2$ times the integer M;

providing a read clock cycle to the read shift register for selected read operations with respect to any of the word storage locations;

in response to each read clock cycle, received from the circuitry for providing the read clock cycle, shifting the sequence in the read shift register;

wherein one bit in the sequence in the read shift register corresponds to an indication of one of the memory word storage locations from which a word will be read; and

evaluating selected bits in the sequence in the write register relative to selected bits in the sequence in the read register for detecting a level of data fullness in the memory structure.

22. The method of claim 21 wherein R_1 equals R_2.

23. The method of claim 22 wherein R_1 and R_2 both equal one.

24. The method of claim 21:

wherein the step of providing a write clock cycle to the write shift register for selected write operations provides a write clock cycle for every R_1 write operations with respect to any of the word storage locations; and

wherein the step of for providing a read clock cycle to the read shift register for selected read operations provides a read clock cycle for every R_2 read operations with respect to any of the word storage locations.

25. The method of claim 21 wherein the step of evaluating selected bits comprises monitoring positioning of the sequence in the write shift register relative to positioning of the sequence in the read shift register.

26. The method of claim 25 wherein the step of evaluating provides a signal in response to detecting that the positioning of the sequence in the write shift register is approaching the positioning of the sequence in the read shift register so as to indicate that the M storage locations are approaching a data full status.

27. The method of claim 25 wherein the step of evaluating provides a signal in response to detecting that the positioning of the sequence in the read shift register is approaching the positioning of the sequence in the write shift register so as to indicate that the M storage locations are approaching a data empty status.

28. The method of claim 25 wherein the step of evaluating provides a signal in response to detecting that the positioning of the sequence in the write shift register relative to the positioning of the sequence in the read shift register indicates that the one of the memory word storage locations into which a word will be written is $M/2$ storage locations away from the one of the memory word storage locations from which a word will be read.

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